ALLAMAIQBALOPENUNIVERSITY,ISLAMABAD

(DepartmentofComputerScience)

WARNING

1. **PLAGIARISM OR HIRING OF GHOST WRITER(S) FOR SOLVING THE ASSIGNMENT(S) WILL DEBARTHESTUDENTFROMAWARDOFDEGREE/CERTIFICATE,IFFOUNDATANYSTAGE.**
2. **SUBMITTINGASSIGNMENTSBORROWEDORSTOLENFROMOTHER(S)ASONE'SOWN WILL BE PENALIZED AS DEFINED IN "AIOU PLAGIARISM POLICY".**

Course: Digital Logic Design (3006) **Semester:Spring2026**
Level: BS

Please read the following instructions for writing your assignments. (AD, BS, BEd, MA/MSc, MED, M. Phil, and PhD)

1. All questions are compulsory and carry equal marks, but within a question, the marks are distributed according to its requirements.
2. Read the question carefully and then answer it according to the requirements of the question.
3. Handwritten scanned assignments are not acceptable.
4. Upload your typed (in Word or PDF format) assignments on or before the due date.
5. Late assignments can't be uploaded to theLMS.
6. Your own analysis and synthesis will be appreciated.
7. Avoid irrelevant discussion/information and reproducing from books, study guides,or allied material.

TotalMarks:100 **PassMarks:50**

ASSIGNMENT-1

(Unit1–4)

Question1:

(a) Convert the following numbers to decimal: **(10)**

i). $(1203)_4$ ii). $(5243)_6$

iii). $(9922)_{14}$ iv). $(248)_9$

(b) Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. **(10)**

i). $11001 - 10010$ ii). $1100 - 111100$

iii). $10101 - 11011$ iv). $1100011 - 10001$

Question2:

(a). Simplify the following Boolean expressions to a minimum number of literals **(10)**

i). $xy + xy'$ ii). $(x + y)(x + y')$

iii). $xyz + x'y + xyz'$ iv) $(x + y)'(x' + y')'$

(b) **. Find the complement of** $F = x'y + yz'$**;Thenshow that** $FF' = 0$ **and** $F + F' = 1$ **(10)**

Question3:

a) Simplify the following Boolean Expressions, using four-variable K-maps (10)

i). $F(w,x,y,z) = \sum(0,2,3,4,6,8,9,12)$

ii). $F(w,x,y,z) = \sum(0,1,2,3,5,8,13)$

(b). Simplify the following Boolean expressions, using four-variable K-maps: (10)

i). $ABC'D' + AB'C + B'C'D' + AB'CD + B'C'D$

ii). $wx'y' + w'x'yz + x'y'z + xyz + y'z'$

Question4:

a. Design a combination circuit with three inputs and one output

(i). The output is 1 when the binary value of the inputs is more than 2. The output is 0 otherwise
(ii). The output is 1 when the binary value of the inputs is not divisible by 3

b. Design a combinational circuit that converts a four-bit Gray code to a four-bit binary number. Implement the circuit with an Exclusive-OR gate **(20)**

Question5:

Design a combinational circuit with **three inputs (A, B, C)** and **one output (F)** for the following independent conditions. For each case, provide the **Truth Table**, the **K-map simplification**, and the **Logic Diagram**.

1. The output F is **1** if the decimal equivalent of the binary input is an **even number greater than 0**. The output is **0** otherwise.
2. The output F is **1** if the number of 1s in the input is **exactly one**. The output is **0** otherwise **(20)**

TotalMarks:100 **PassMarks:50**

ASSIGNMENT-2

(Unit5–9)

Question1:.

Assuming you are using D Flip-Flops for the memory elements:

1. State Assignment: Assign binary codes to your states (e.g.,S_0 = 00,S_1= 01, etc.).
2. Excitation Equations: Use Karnaugh Maps (K-Maps) to derive the simplified Boolean expressions for the Flip-Flop inputs (D_1, D_0) and the output (z).
3. Logic Diagram: Sketch the final circuit showing the gates and the two D Flip-Flops. **(20)**

Question2:

Construct and simulate a synchronous 4-bit binary counter **(20)**

Question3:
Design a 4-bit shift register that shifts right on every clock pulse with a serial input of 1. Draw the circuit and show the state of all bits for the first four clock cycles, starting from 0000 **(20)**

Question4:
Compare the power consumption and propagation delay of a CMOS vs. a TTL D-flip-flop as the clock frequency increases. Which technology is more efficient for high-speed sequential operations, and why? **(20)**

Question5:
Design a 4-bit asynchronous counter with a T-flip flop and write its Verilog HDL Code. **(20)**